Amendment Approved 10/20/04 JMK

IN THE SPECIFICATION

Please amend the paragraph at page 7, lines 18-36, as follows:

With the above described construction, it is possible to surely recognize which region of the processor circuit 1, storage circuit 2 and peripheral circuit 3, which are operating in the system LSI, has a bug and which operation process causes the bug, on the basis of the assignment of the place by the selection signal and the output contents of the result signal, so that it is possible to provide an excellent debug function. Furthermore, the selection signal is obtained by simply taking out a predetermined result signal, which is outputted from the outside to a specific region of each internal component circuit via an input pin of the system LSI, to the outside via the selection means 30. The ~~selection~~ control means ~~30~~ 4 does not carry out any special control operations, and is designed to output a selection signal, which is inputted only to assign a place to be monitored, to the selection means ~~33~~ 30 so as to be able to assign a place, in which the selection means ~~33~~ 30 can output a result signal from any operation process in any place of internal component circuits, and an operation stage in any operation process.

Please amend the paragraph at page 14, lines 22-25, as follows:

Furthermore, a signal ~~tinning-out~~ thinning-out circuit for substantially lowering the frequency (data rate) of at least one of the output signals of the first and second signal selection circuits 31 and 32 shown in FIG. 11 may be provided.

Please amend the paragraph at page 15, lines 4-11, as follows:

In the above described preferred embodiments, while the values of the program counter 11 in the MPU core 1, accumulator 12 and various registers 13 have been selected by the signal selection circuit, the concrete circuit block for analyzing the internal state of the MPU core 1 should not particularly ~~been~~ be limited. Similarly, the concrete circuit block for analyzing the internal state of the peripheral circuit 3 should not particularly be limited.